Elimination of Charge Sharing Problem in Dynamic Circuit

Saurabh Sharma, Sr.Lecturer, Department of Electronics and Communication, MIET Group, Meerut
Sanjeev Maheshwari, Director, MIET Group, Meerut
Sanjeev Kumar, HOD, Department of Electrical Engineering, IET Group, Meerut
Vrince Vimal, Asst. Professor, Department of Electronics and Communication, MIET Group, Meerut

ABSTRACT
A technology is proposed in this literature to simultaneously reduce the charge sharing problem in the dynamic circuits due to the generation of the parasitic capacitor at each node. Here we used a weak PMOS pull-up device (with a small W/L ratio) to the dynamic CMOS stage output to reduce the effect of the parasitic capacitor.

Keywords—NMOS, PMOS, CMOS, domino logic, weaker PMOS.

Tool Used---- Tanner.

Introduction
The digital integrated circuit charge sharing problem has become one of the foremost issues in the design of very deep submicron VLSI chips. Charge sharing in digital circuits refers to any phenomenon that causes the voltage at a node to deviate from its nominal value. While these charge sharing always existed, in the past they had little impact on the performance of integrated circuits and were often neglected. It is the unstopped aggressive technology scaling in an effort to continuously improve chip performance and integration level that makes charge sharing plays an increasingly important role in comparison with conventional design metrics like area, speed and power consumption.

Together with technology scaling, aggressive design practices like employing dynamic logic styles have also seen wider use in recent years to achieve higher performance of integrated circuits. Circuits design using dynamic logic style can be considerably faster and more compact then their static CMOS counterparts. This is especially the case with wide fan-in dynamic logic gates where a single gate can realize the logic function that otherwise would require multiple levels of static CMOS logic gates. Therefore, wide fan-in dynamic gates are routinely employed in performance-critical blocks of high performance chips, such as in microprocessor, digital signal processor, and so on.

In this paper, we propose a novel design method to enhance the charge sharing problem tolerance of dynamic circuits by analyzes their results on tanner. We will show that dynamic logic gates are not necessarily less charge sharing problem tolerant if proper charge sharing problem tolerant design techniques are employed. In fact, using the proposed method in this paper, charge sharing tolerance of dynamic logic circuits can be improved beyond the level of static CMOS logic gates while still retain their advantage in performance. The proposed charge sharing tolerant design method can be realized using a number of different circuits and therefore having broader impact.

Dynamic Circuit
In the dynamic CMOS circuit technique, clock pulse is given between a PMOS and a NMOS and the NMOS logic is connected between them. The circuit operation is based on first precharging the output node capacitance and subsequently evaluating the output level according to the applied inputs. Both of these operations are scheduled by a single clock signal which drives one NMOS and one PMOS transistors in each dynamic stage.

When the clock signal is high then precharge transistor p1 turns off and n1 turns on. If the input signal creates a conducting path between the output node and ground then output capacitance will discharge towards 0V. When the clock signal is low the PMOS transistor p1 is conducting and the complementary NMOS transistor n1 is off. The output capacitance of the circuit is charged up through the conducting PMOS transistor to a logic high level of VDD.
Fig. 1: CMOS Dynamic inverter

Above we have implemented the dynamic inverter using tanner and generated its waveform. Fig. 2 shows that there is a problem in dynamic circuit, in the evaluation phase if the input is low the capacitance is already charge to VDD but due to the charge distribution at each node of NMOS logic, it will be corrupted.

Fig. 2: Waveform for CMOS dynamic inverter
Domino logic

In the domino logic, we connected a static CMOS inverter at the output of the dynamic circuit. During the precharge phase (when clock is 0), the output node of the dynamic CMOS stage is precharged to high logic level, and the output of the CMOS inverter becomes low. When the clock signal rises at the beginning of the evaluation phase, there are two possibilities: The output node of the dynamic CMOS stage is either discharged to low level through the NMOS circuitry (1 to 0 transition), or it remains high. Consequently, the inverter output voltage can also make at most one transition during the evaluation phase, from 0 to 1. Regardless of the input voltage applied to the dynamic CMOS stage, it is not possible for the CMOS inverter to make a 1 to 0 transition during the evaluation phase.

![Diagram of Domino Logic](image)

Fig.3: Domino logic

Above we have implemented the domino logic using Tanner and generated its waveform. Fig.4 shows that there are some limitations in the domino logic. First, only non-inverting structure can be implemented and second charge sharing between the dynamic stage output node and the intermediate nodes of the NMOS logic block during the evaluation phase may cause erroneous outputs.

![Waveform for Domino Logic](image)

Fig.4: Waveform for domino logic
Removal Of Charge Sharing Problem
Using Weak PMOS Logic

One simple solution to remove charge sharing problem is just to add a weak PMOS pull-up device (with a small W/L ratio) to the dynamic CMOS stage output, which essentially forces a high output level unless there is a strong pull-down path between the output and the ground. It can be observed that the weak PMOS transistor will be turned on only when the precharge node voltage is kept high. Otherwise it will be turned off as output voltage becomes high.

Fig.5: Weaker PMOS logic

Above we have implemented an inverter with weak PMOS using tanner and generated its waveform. As we can see the waveform is sharp at both rising and falling edges and there is no charge sharing problem.

Fig.6: Waveform for weaker PMOS logic
Results and Conclusions
By analyzing the above circuits on the tanner we conclude that the charge sharing problem in the dynamic circuit can be improve by adding a weak PMOS pull-up device to the dynamic CMOS stage output.

References